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... The synthesized **circuit** contains over 1200 single-event **...** among Functional Blocks Another **static analysis** that can ... dynamic path **analysis** or **timing** simulation is a **...**
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A 30-MHz hybrid analog/digital clock recovery **circuit** in 2-μ mCMOS
B Kim, DN Helman, PR Gray - Solid-State Circuits, IEEE Journal of, 1990 - ieeexplore.ieee.org
... a second-order loop with zero **static** phase error **...** KIM et al.: HYBRID ANALOG/DIGITAL CLOCK RECOVERY **CIRCUIT ...** A first-order **analysis** of thermal noise accumulation **...**
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... because it causes the worst **timing** delay and ... get the total expected current waveform for the **circuit**. ... For **static** signal probabilities (as opposed to probability ...
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Estimation of maximum current envelope for power bus **analysis** and design
S Bobba, IN Hajj - Proceedings of the 1998 international symposium on Physical ..., 1998 - portal.acm.org
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WE Donath, RB Hitchcock, JP Soreff - US Patent 5,365,463, 1994 - freepatentsonline.com
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S Rotem, K Stevens, R Ginosar, P Beerel, C Myers, ... - Proc. International Symposium on Advanced Research in ..., 1999 - doi.ieeecs.org
... self-timed circuits using any future **circuit** or **implementation** ... The design uses **static** and domino gates from ... to noise on **control** lines, **timing** verification, and ...
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